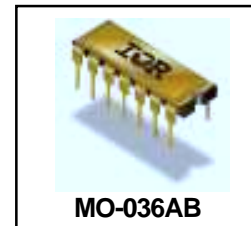


**RADIATION HARDENED 100V, Combination 2N-2P-CHANNEL
 POWER MOSFET
 THRU-HOLE (MO-036AB)**

IRHG6110
RAD-Hard™ HEXFET®
MOSFET TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	Id	CHANNEL
IRHG6110	100K Rads (Si)	0.6Ω	1.0A	N
IRHG63110	300K Rads (Si)	0.6Ω	1.0A	N
IRHG6110	100K Rads (Si)	1.1Ω	-0.75A	P
IRHG63110	300K Rads (Si)	1.1Ω	-0.75A	P



International Rectifier's RAD-Hard™ HEXFET® MOSFET Technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Proton Tolerant
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Package
- Light Weight

Absolute Maximum Ratings (Per Die)

Pre-Irradiation

	Parameter	N-Channel	P-Channel	Units
ID @ VGS = ± 12V, TC = 25°C	Continuous Drain Current	1.0	-0.75	A
ID @ VGS = ± 12V, TC = 100°C	Continuous Drain Current	0.6	-0.5	
IDM	Pulsed Drain Current ①	4.0	-3.0	
PD @ TC = 25°C	Max. Power Dissipation	1.4	1.4	W
	Linear Derating Factor	0.011	0.011	W/°C
VGS	Gate-to-Source Voltage	±20	±20	V
EAS	Single Pulse Avalanche Energy	56 ②	75 ③	mJ
IAR	Avalanche Current ①	1.0	-0.75	A
EAR	Repetitive Avalanche Energy ①	0.14	0.14	mJ
dv/dt	Peak Diode Recovery dv/dt	2.4 ③	2.4 ④	V/ns
TJ	Operating Junction	-55 to 150		°C
TSTG	Storage Temperature Range			
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)		
	Weight	1.3 (Typical)		g

For footnotes refer to the last page

Electrical Characteristics For Each N-Channel Device @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
B _V DSS	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 1.0mA
ΔB _V DSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.125	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.7	Ω	V _{GS} = 12V, I _D = 1.0A ④
		—	—	0.6		V _{GS} = 12V, I _D = 0.6A
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 1.0mA
g _{fs}	Forward Transconductance	0.7	—	—	S (ℓ)	V _{DS} > 15V, I _{DS} = 0.6A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	—	11	nC	V _{GS} = 12V, I _D = 1.0A, V _{DS} = 50V
Q _{gs}	Gate-to-Source Charge	—	—	3.0		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	4.0		
t _{d(on)}	Turn-On Delay Time	—	—	20	ns	V _{DD} = 50V, I _D = 1.0A, V _{GS} = 12V, R _G = 7.5Ω
t _r	Rise Time	—	—	16		
t _{d(off)}	Turn-Off Delay Time	—	—	65		
t _f	Fall Time	—	—	45		
L _S + L _D	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C _{iss}	Input Capacitance	—	300	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	100	—		
C _{rss}	Reverse Transfer Capacitance	—	16	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.0	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	4.0		
V _{SD}	Diode Forward Voltage	—	—	1.5	V	T _j = 25°C, I _S = 1.0A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	—	110	nS	T _j = 25°C, I _F = 1.0A, di/dt ≤ 100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	390	nC	V _{DD} ≤ 25V ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	17	°C/W	Typical socket mount
R _{thJA}	Junction-to-Ambient	—	—	90		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @ T_j = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BVDSS	Drain-to-Source Breakdown Voltage	-100	—	—	V	V _{GS} = 0V, I _D = -1.0mA
ΔBVDSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	-0.11	—	V/°C	Reference to 25°C, I _D = -1.0mA
RDS(on)	Static Drain-to-Source On-State Resistance	—	—	1.2	Ω	V _{GS} = -12V, I _D = -0.75A ^④
		—	—	1.1		V _{GS} = -12V, I _D = -0.5A
VGS(th)	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -1.0mA
gfs	Forward Transconductance	0.6	—	—	S (Ω)	V _{DS} > -15V, I _{DS} = -0.5A ^④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	-25	μA	V _{DS} = -80V, V _{GS} = 0V
		—	—	-250		V _{DS} = -80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V _{GS} = 20V
Q _g	Total Gate Charge	—	—	15	nC	V _{GS} = -12V, I _D = -0.75A, V _{DS} = -50V
Q _{gs}	Gate-to-Source Charge	—	—	4.0		
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	4.3		
t _{d(on)}	Turn-On Delay Time	—	—	22	ns	V _{DD} = -50V, I _D = -0.75A, V _{GS} = -12V, R _G = 24Ω
t _r	Rise Time	—	—	19		
t _{d(off)}	Turn-Off Delay Time	—	—	66		
t _f	Fall Time	—	—	51		
LS + LD	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C _{iss}	Input Capacitance	—	335	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	100	—		
C _{rss}	Reverse Transfer Capacitance	—	22	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-0.75	A	
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	-3.0		
V _{SD}	Diode Forward Voltage	—	—	-2.5	V	T _j = 25°C, I _S = -0.75A, V _{GS} = 0V ^④
t _{rr}	Reverse Recovery Time	—	—	90	nS	T _j = 25°C, I _F = -0.75A, di/dt ≤ -100A/μs
Q _{RR}	Reverse Recovery Charge	—	—	257	nC	V _{DD} ≤ -25V ^④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by LS + LD.				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJC}	Junction-to-Case	—	—	17	°C/W	Typical socket mount
R _{thJA}	Junction-to-Ambient	—	—	90		

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each N-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si) ¹		300K Rads (Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V _{GS} = 0V, I _D = 1.0mA
V _{GS(th)}	Gate Threshold Voltage	2.0	4.0	1.25	4.5		V _{GS} = V _{DS} , I _D = 1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	—	100	nA	V _{GS} = 20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100	—	-100		V _{GS} = -20V
I _{DSS}	Zero Gate Voltage Drain Current	—	25	—	25	μA	V _{DS} = 80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (TO-39)	—	0.56	—	0.66	Ω	V _{GS} = 12V, I _D = 0.6A
R _{DS(on)}	Static Drain-to-Source ^④ On-State Resistance (MO-036AB)	—	0.60	—	0.70	Ω	V _{GS} = 12V, I _D = 0.6A
V _{SD}	Diode Forward Voltage ^④	—	1.5	—	1.5	V	V _{GS} = 0V, I _S = 1.0A

1. Part number IRHG6110
2. Part number IRHG63110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area (Per Die)

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@ V _{GS} =0V	@ V _{GS} =-5V	@ V _{GS} =-10V	@ V _{GS} =-15V	@ V _{GS} =-20V
Cu	28.0	285	43.0	100	100	100	80	60
Br	36.8	305	39.0	100	90	70	50	—

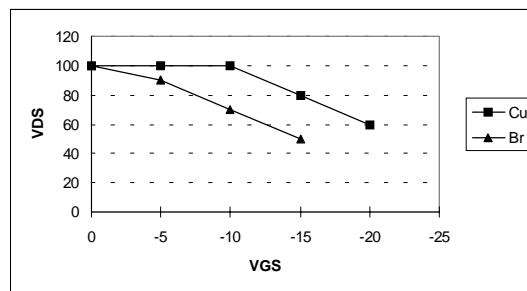


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

Radiation Characteristics

IRHG6110

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each P-Channel Device @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads(Si) ¹		300K Rads (Si) ²		Units	Test Conditions
		Min	Max	Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	-100	—	-100	—	V	V _{GS} = 0V, I _D = -1.0mA
V _{GS(th)}	Gate Threshold Voltage	- 2.0	- 4.0	-2.0	-5.0		V _{GS} = V _{DS} , I _D = -1.0mA
I _{GSS}	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V _{GS} = -20V
I _{GSS}	Gate-to-Source Leakage Reverse	—	100	—	100		V _{GS} = 20 V
I _{DSS}	Zero Gate Voltage Drain Current	—	-25	—	-25	μA	V _{DS} =-80V, V _{GS} =0V
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	1.06	—	1.06	Ω	V _{GS} = -12V, I _D =-0.5A
R _{DS(on)}	Static Drain-to-Source ④ On-State Resistance (MO-036AB)	—	1.1	—	1.1	Ω	V _{GS} = -12V, I _D =-0.5A
V _{SD}	Diode Forward Voltage ④	—	-2.5	—	-2.5	V	V _{GS} = 0V, I _S = -0.75A

1. Part number IRHG6110

2. Part number IRHG63110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area (Per Die)

Ion	LET MeV/(mg/cm ²)	Energy (MeV)	Range (μm)	V _{DS} (V)				
				@ V _{GS} =0V	@ V _{GS} =5V	@ V _{GS} =10V	@ V _{GS} =15V	@ V _{GS} =20V
Cu	28.0	285	43.0	-100	-100	-100	-70	-60
Br	36.8	305	39.0	-100	-100	-70	-50	-40
I	59.8	343	32.6	-60	—	—	—	—

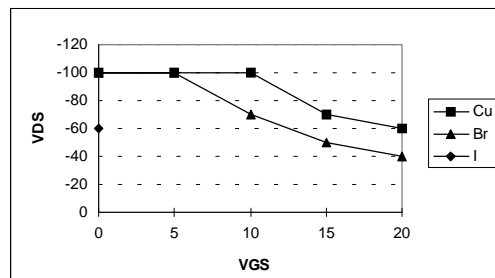


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

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5

N-Channel
Q1,Q3

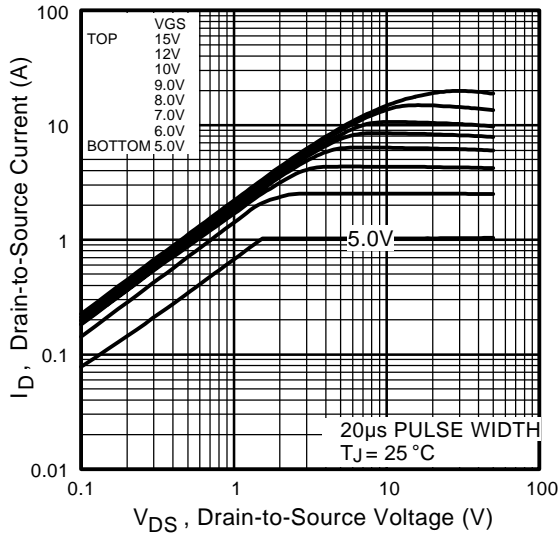


Fig 1. Typical Output Characteristics

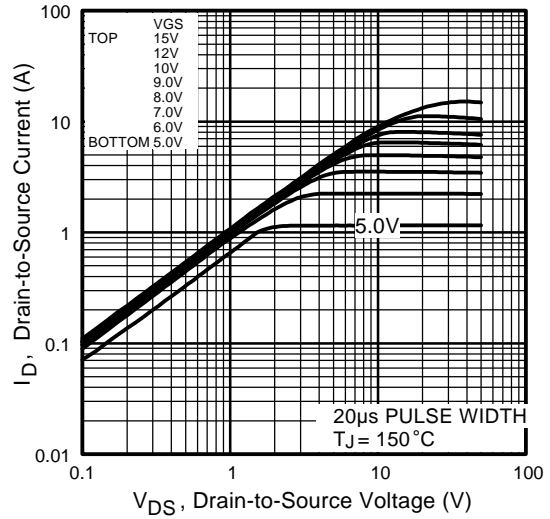


Fig 2. Typical Output Characteristics

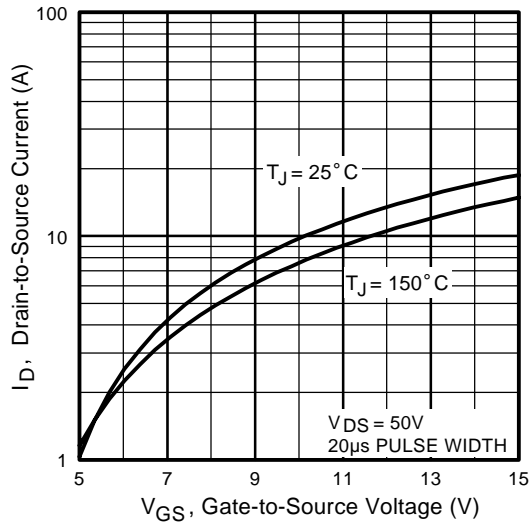


Fig 3. Typical Transfer Characteristics

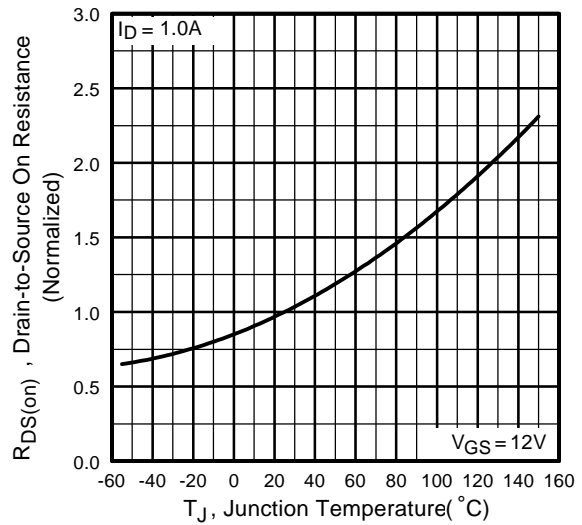


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel
Q1,Q3

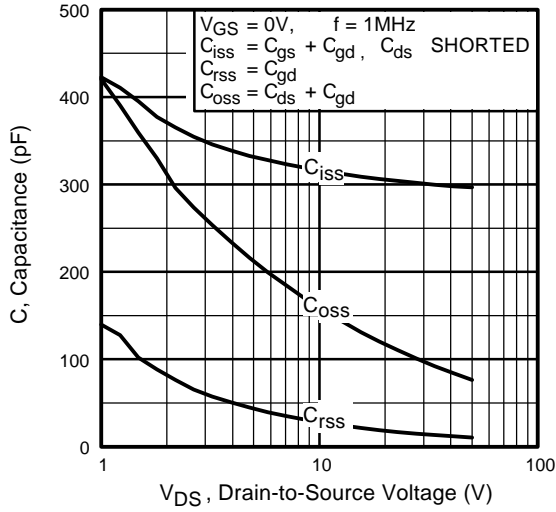


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

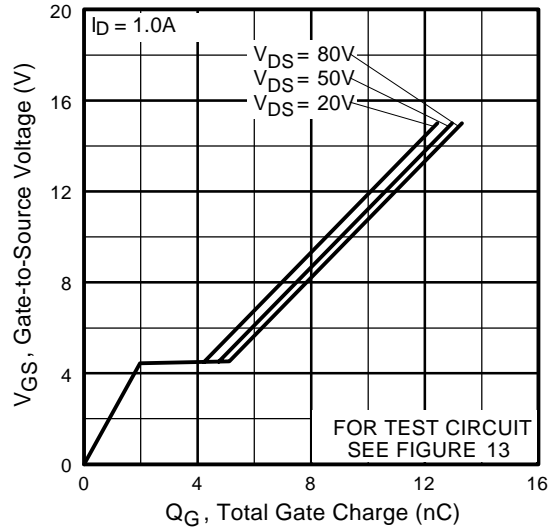


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

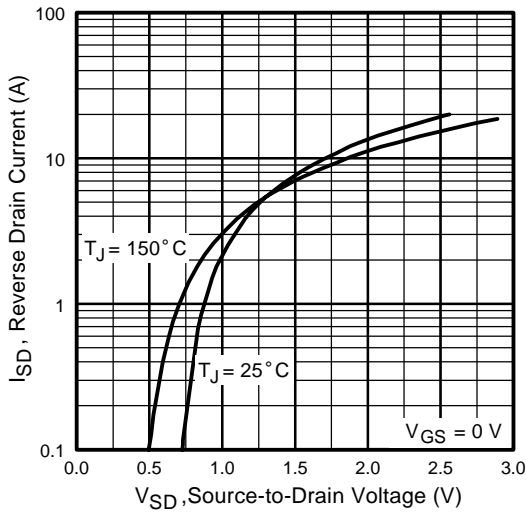


Fig 7. Typical Source-Drain Diode Forward Voltage

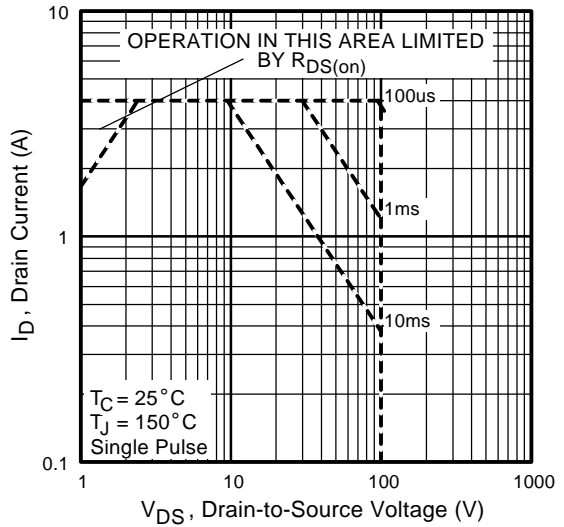


Fig 8. Maximum Safe Operating Area

N-Channel
Q1,Q3

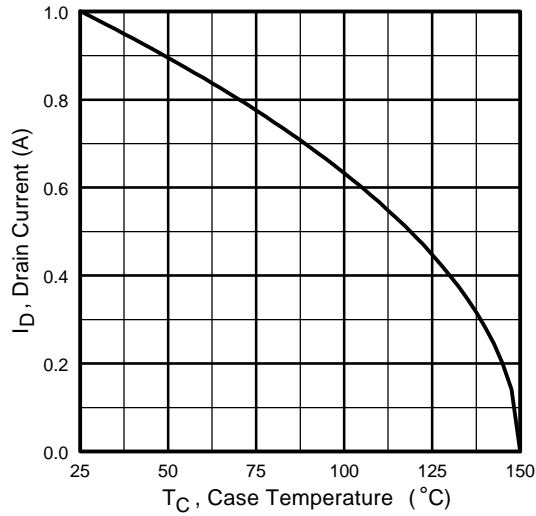


Fig 9. Maximum Drain Current Vs. Case Temperature

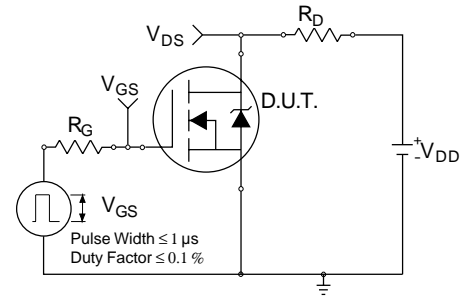


Fig 10a. Switching Time Test Circuit

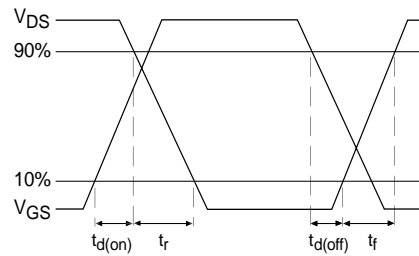


Fig 10b. Switching Time Waveforms

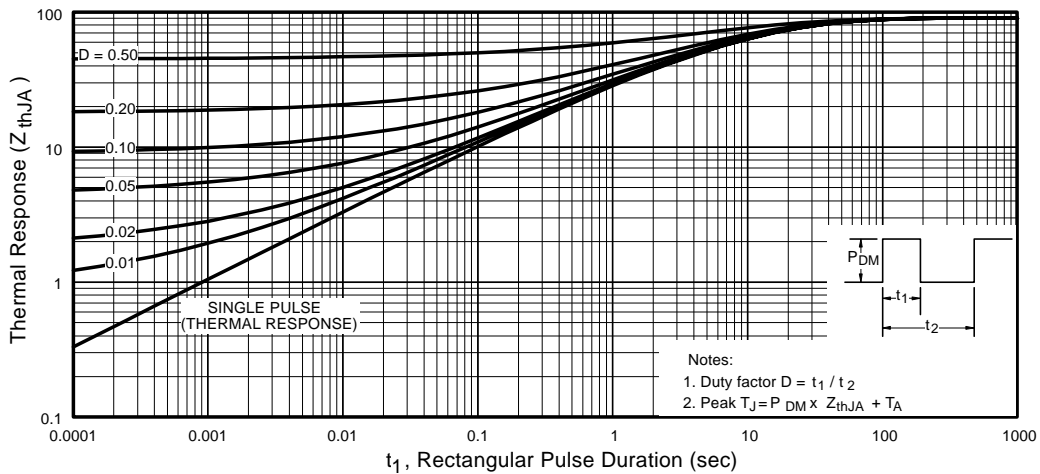


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

N-Channel
Q1,Q3

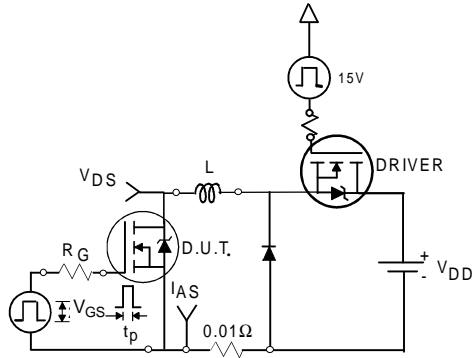


Fig 12a. Unclamped Inductive Test Circuit

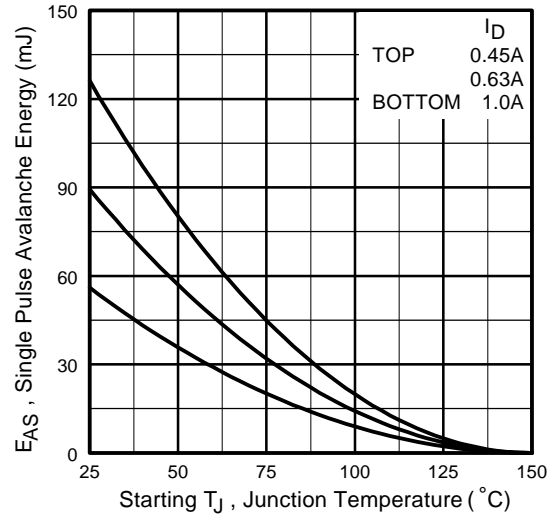


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

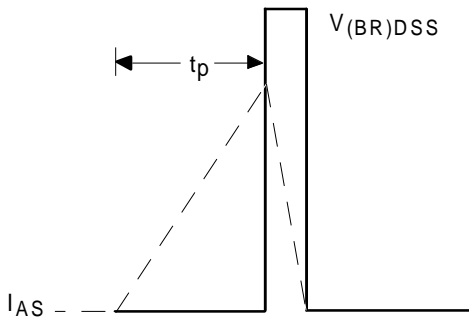


Fig 12b. Unclamped Inductive Waveforms

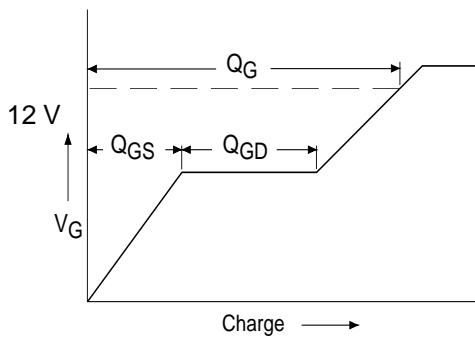


Fig 13a. Basic Gate Charge Waveform

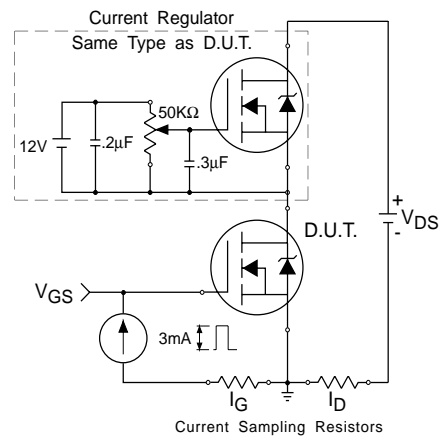


Fig 13b. Gate Charge Test Circuit

**P-Channel
Q2,Q4**

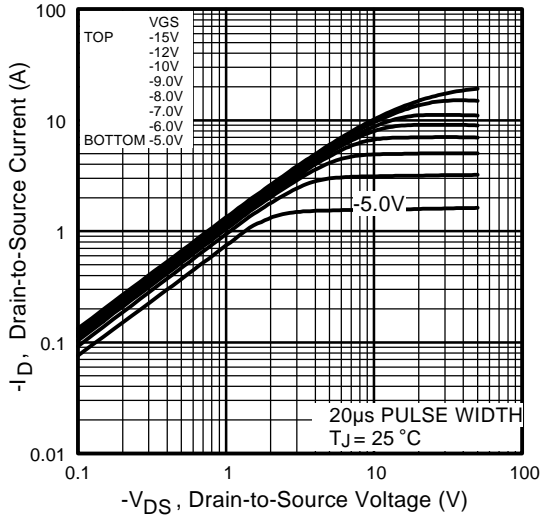


Fig 1. Typical Output Characteristics

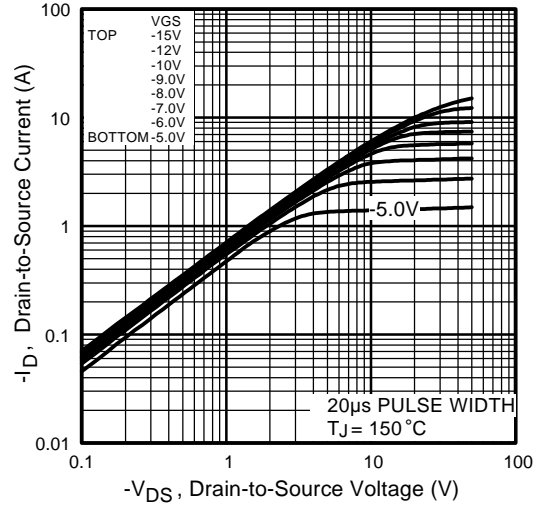


Fig 2. Typical Output Characteristics

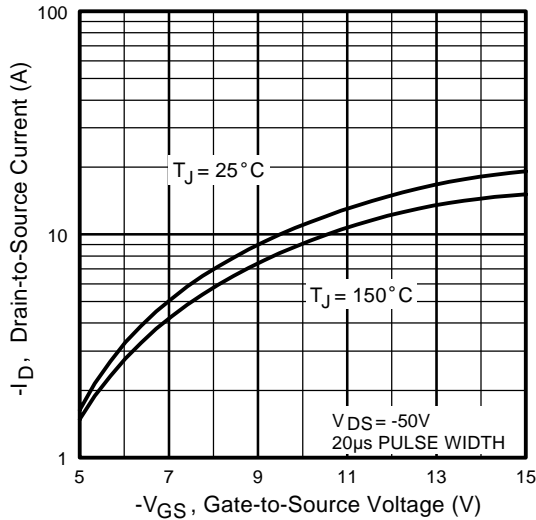


Fig 3. Typical Transfer Characteristics

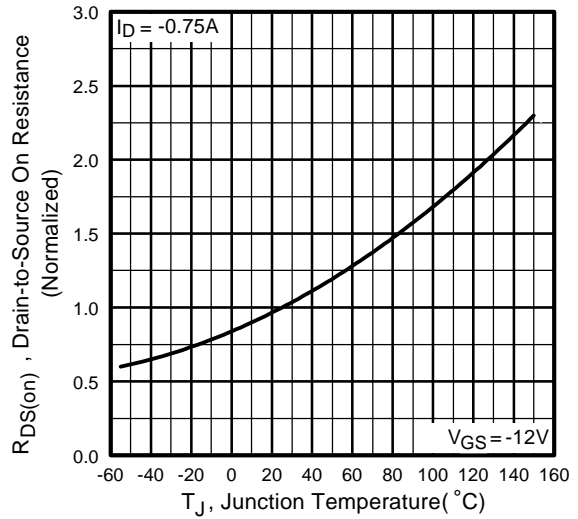


Fig 4. Normalized On-Resistance Vs. Temperature

P-Channel
Q2,Q4

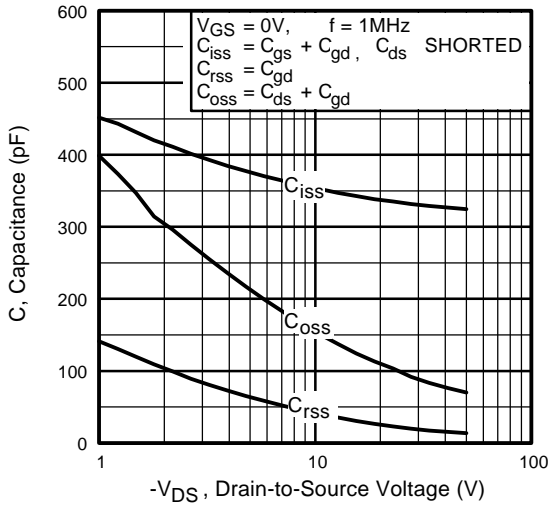


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

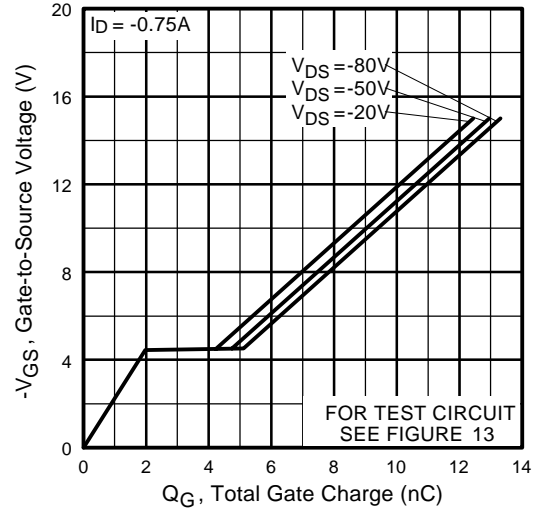


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

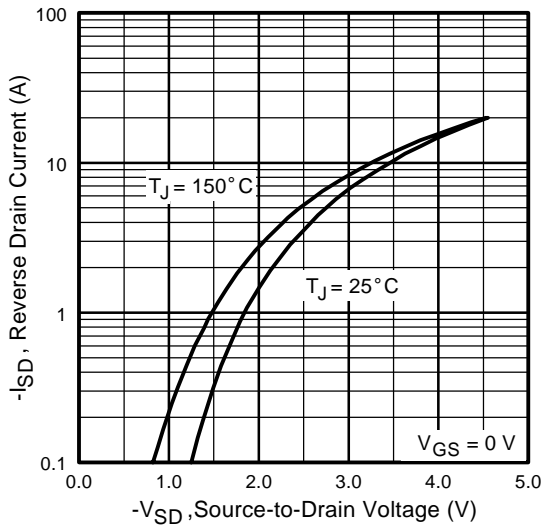


Fig 7. Typical Source-Drain Diode Forward Voltage

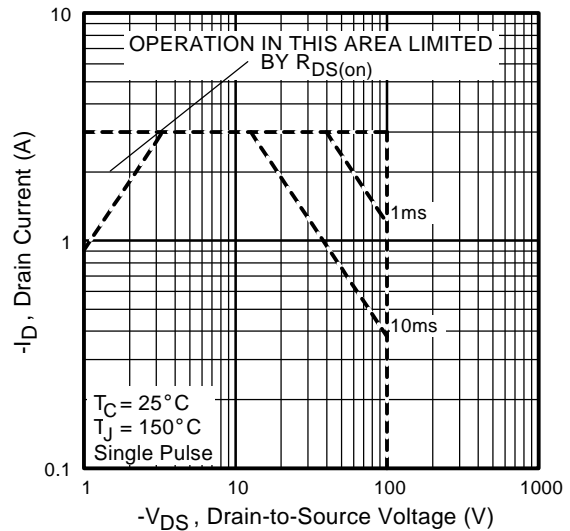


Fig 8. Maximum Safe Operating Area

P-Channel
Q2,Q4

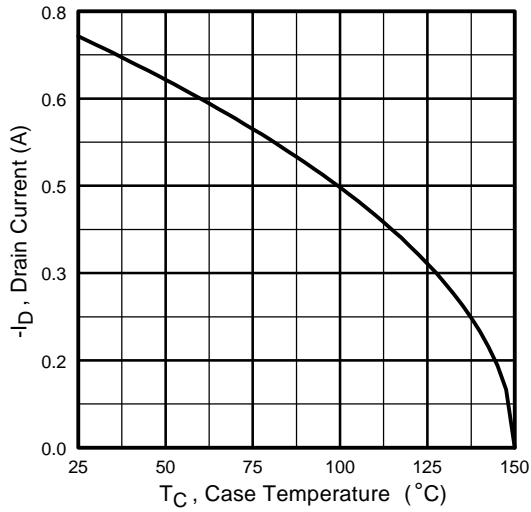


Fig 9. Maximum Drain Current Vs. Case Temperature

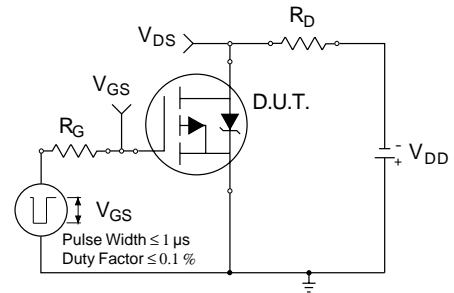


Fig 10a. Switching Time Test Circuit

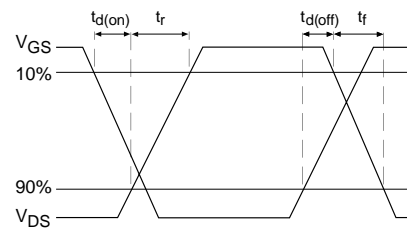


Fig 10b. Switching Time Waveforms

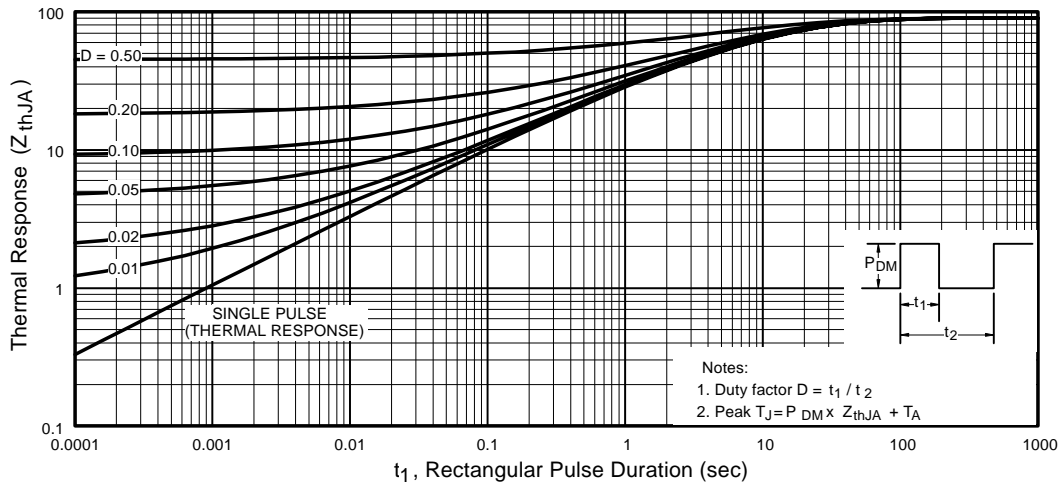


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

**P-Channel
Q2,Q4**

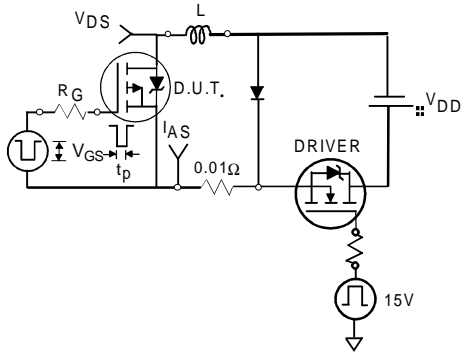


Fig 12a. Unclamped Inductive Test Circuit

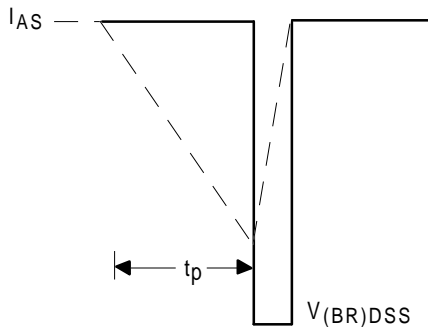


Fig 12b. Unclamped Inductive Waveforms

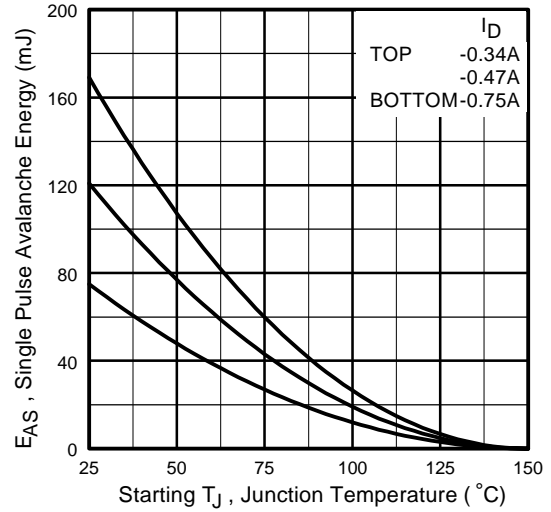


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

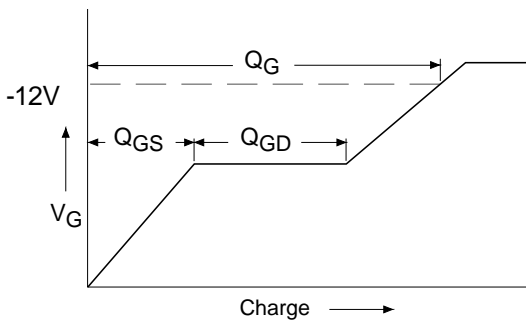


Fig 13a. Basic Gate Charge Waveform

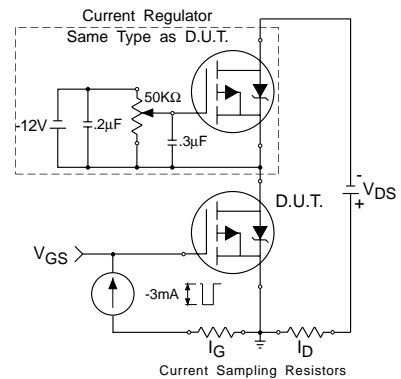


Fig 13b. Gate Charge Test Circuit

